查询SAA5244供应商

DATA SHEET

SAA5244A
Integrated VIP and teletext decoder (IVT1.1)

Product specification
File under Integrated Circuits, IC02

March 1992

Philips Semiconductors

PHILIPS

Integrated VIP and teletext decoder (IVT1.1)

SAA5244A

FEATURES

- Complete teletext decoder including page memory in a single 40-pin DIL package
- Single +5 V power supply
- Digital data slicer and display clock phase-locked loop reduces peripheral components to a minimum
- Both video and scan related synchronization modes are supported
- On board single page memory including extension packets for FASTEXT
- Single page acquisition system
- RGB interface to standard colour decoder ICs, push-pull output drive
- Data capture performance similar to SAA5231 (VIP2)
- Simple software control via I^{2}C-bus
- Option for five national languages
- 32 supplementary characters for on-screen displays
- Optional storage of packet 24 in the display memory
- Page links in packets 27 and 8/30 are Hamming decoded
- Separate text and video signal quality detectors, 625/525 video status and language version all readable via I^{2}C-bus
- Automatic ODD/$\overline{\text{EVEN}}$ output control with manual override
- Control of display PLL free-run and rolling header via I^{2}C-bus
- VCS to SCS mode for stable 525 line status display

DESCRIPTION

The Integrated VIP and Teletext (IVT1.1) is a teletext decoder (contained within a single-chip package) for decoding 625-line based World System Teletext transmissions. The teletext decoder hardware is based on a reduced function version of the device SAA5246 (IVT1.0).

The Video Input Processor (VIP) section of the device uses mixed analog and digital designs for the data slicer and the display clock phase-locked loop functions. As a result the number of external components is greatly reduced and no critical or adjustable components are required. A single page static RAM is incorporated in the device thereby giving a genuine single-chip teletext decoder device.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA5244AP	40	DIL	plastic	SOT129(1)
SAA5244AGP	44	QFP	plastic	SOT205A(2)

Notes

1. SOT129-1; 1996 December 16.
2. SOT205-1; 1996 December 16.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	4.5	5	5.5	V
I_{DD}	supply current	–	74	148	mA
V_{syn}	sync amplitude	0.1	0.3	0.6	V
V_{vid}	video amplitude	0.7	1	1.4	V
f_{XTAL}	crystal frequency	–	27	–	MHz
T_{amb}	operating ambient temperature range	–20	–	70	°C

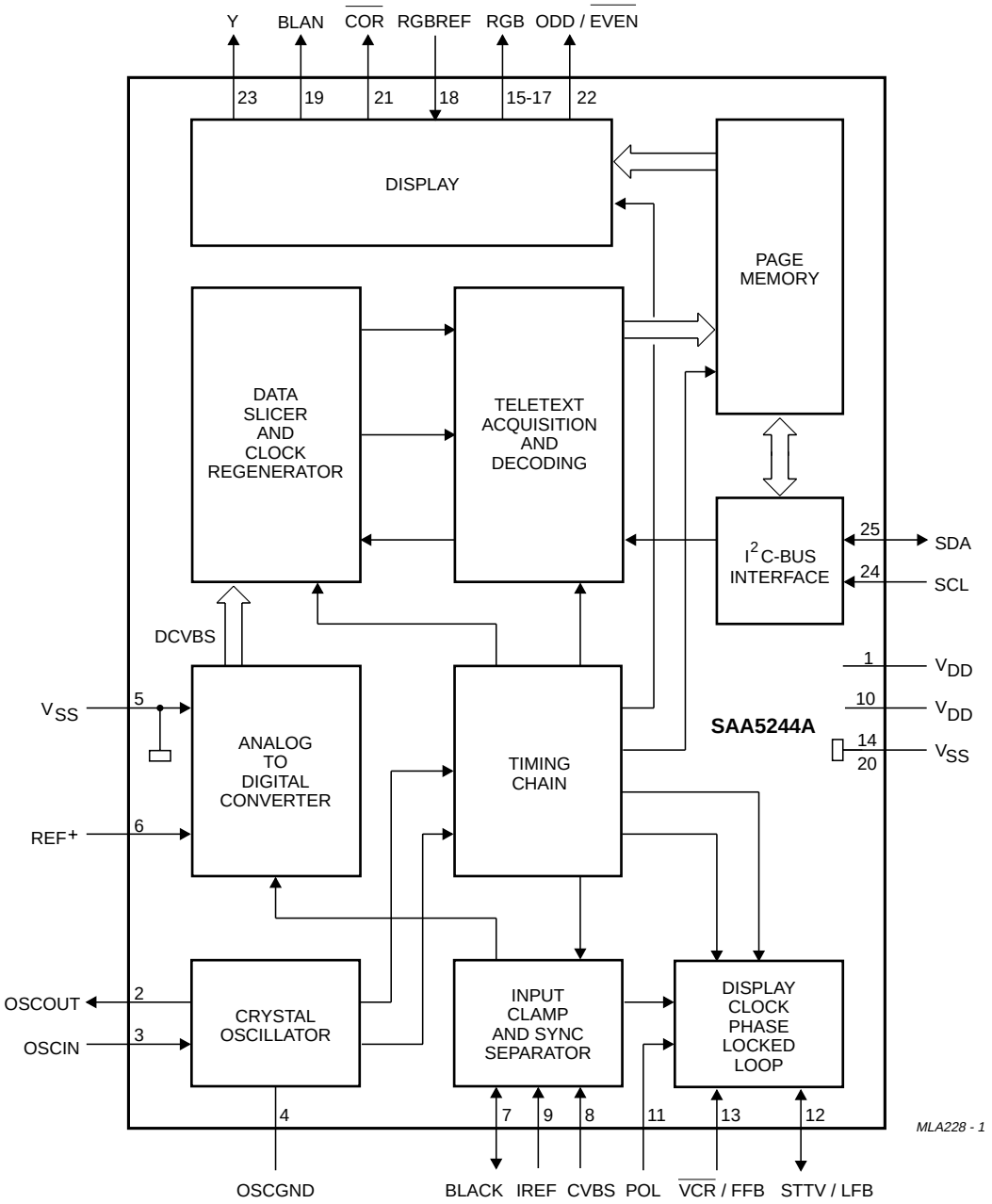


Fig.1 Block diagram for SOT129 (DIL40) package.

PINNING

SYMBOL	SOT129	SOT205A	DESCRIPTION
V_{DD}	1	18	+5 V supply
OSCOUT	2	19	27 MHz crystal oscillator output
OSCIN	3	20	27 MHz crystal oscillator input
OSCGND	4	21	0 V crystal oscillator ground
V_{SS}	5	22	0 V ground
REF–	–	–	negative reference voltage for the ADC. The pin should be connected to 0 V
REF+	6	23	positive reference voltage for the ADC. The pin should be connected to +5 V
BLACK	7	24	video black level storage pin, connected to ground via a 100 nF capacitor
CVBS	8	25	composite video input pin. A positive-going 1 V (peak-to-peak) input is required, connected via a 100 nF capacitor
IREF	9	26	reference current input pin, connected to ground via a 27 kΩ resistor
V_{DD}	10	27	+5 V supply
POL	11	28	STTV/LFB/FFB polarity selection pin
STTV/LFB	12	29	sync to TV output pin/line flyback input pin. Function controlled by an internal register bit (scan sync mode)
$\overline{\text{VCR}}$/FFB	13	32	PLL time constant switch/field flyback input pin. Function controlled by an internal register bit (scan sync mode)
V_{SS}	14	33	0 V ground
R	15	34	dot rate character output of the RED colour information
G	16	35	dot rate character output of the GREEN colour information
B	17	36	dot rate character output of the BLUE colour information
RGBREF	18	37	input DC voltage to define the output high level on the RGB pins
BLAN	19	38	dot rate fast blanking output
V_{SS}	20	39	0 V ground
$\overline{\text{COR}}$	21	40	programmable output to provide contrast reduction of the TV picture for mixed text and picture displays or when viewing newsflash/subtitle pages; open drain output
ODD/$\overline{\text{EVEN}}$	22	41	25 Hz output synchronized with the CVBS input's field sync pulses to produce a non-interlaced display by adjustment of the vertical deflection currents
Y	23	42	dot rate character output of teletext foreground colour information open drain output
SCL	24	43	serial clock input for the I^2C-bus. It can still be driven during power-down of the device
SDA	25	44	serial data port for the I^2C-bus; open drain output. It can still be driven during power-down of the device
n.c.	–	4 to 7 30, 31	not connected
i.c.	26 to 40	1 to 3 8 to 17	internally connected. Must be left open-circuit in application

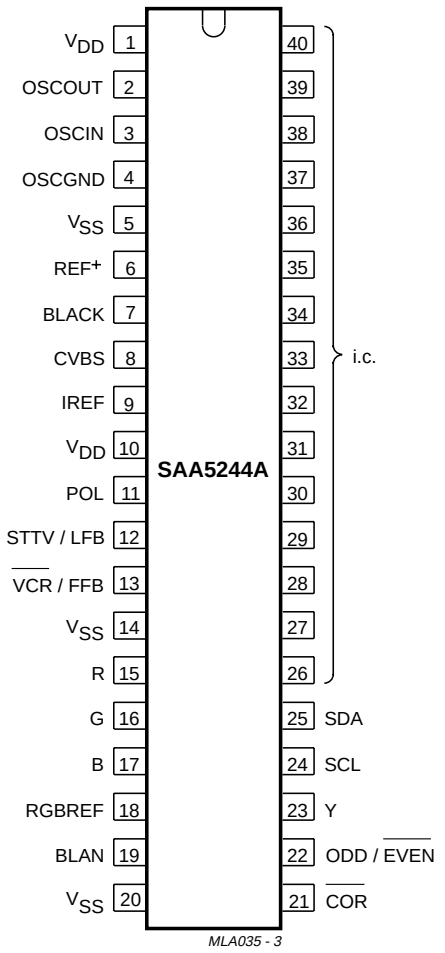


Fig.2 Pin configuration; SOT129 (DIL40).

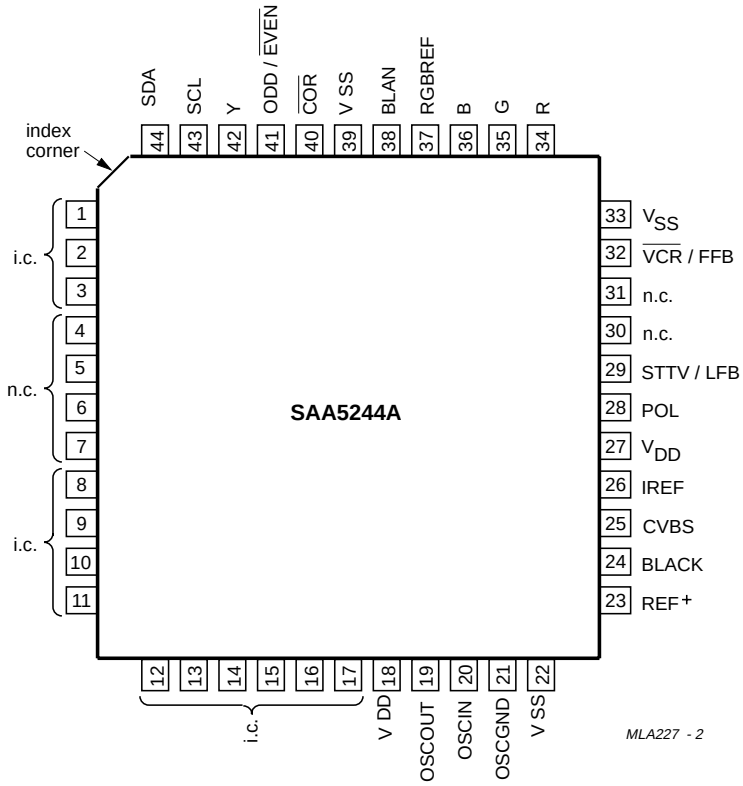


Fig.3 Pin configuration; SOT205A (QFPL44).

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage (all supplies)	–0.3	6.5	V
V_I	input voltage (any input)	–0.3	V_{DD}+0.5	V
V_O	output voltage (any output)	–0.3	V_{DD}+0.5	V
I_O	output current (each output)	–	±10	mA
I_{IOK}	DC input or output diode current	–	±20	mA
T_{amb}	operating ambient temperature range	–20	70	°C
T_{stg}	storage temperature range	–55	125	°C
V_{stat}	electrostatic handling human body model (note 1)	 –2000	 2000	 V

Note

1. The human body model ESD simulation is equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor; this produces a single discharge transient. Reference Philips Semiconductors test method UZW-B0/FQ-A302 (compatible with MIL-STD method 3015.7).

Failure Rate

The failure rate at T_{amb} = 55 °C will be a maximum of 1000 FITS (1 FIT = 1 x 10^{-9} failures per hour).

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = –20 to +70 °C, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage range (V_{DD}–V_{SS})		4.5	5	5.5	V
I_{DD}	total supply current		–	74	148	mA
Inputs						
CVBS						
V_{syn}	sync amplitude		0.1	0.3	0.6	V
t_{syn}	delay from CVBS to TCS output from STTV buffer (nominal video, average of leading/trailing edge)		–150	0	150	ns
t_{syd}	change in sync delay between all black and all white video input at nominal levels		0	–	25	ns
$V_{vid(p-p)}$	video input amplitude (peak-to-peak)		0.7	1	1.4	V
	display PLL catching range		±7	–	–	%
Z_{src}	source impedance		–	–	250	Ω
C_I	input capacitance		–	–	10	pF
IREF						
R_g	resistor to ground		–	27	–	kΩ
POL						
V_{IL}	input voltage LOW		–0.3	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
C_I	input capacitance		–	–	10	pF
LFB						
V_{IL}	input voltage LOW		–0.3	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
I_I	input current	note 1	–1	–	1	mA
t_{LFB}	delay between LFB front edge and input video line sync		–	250	–	ns
$\overline{VCR}$/FFB						
V_{IL}	input voltage LOW		–0.3	–	0.8	V
V_{IH}	input voltage HIGH		2.0	–	V_{DD}+.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
I_I	input current	note 1	–1	–	1	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
RGBREF (NOTE 2)						
V_I	input voltage		–0.3	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
I_{DC}	DC current		–	–	10	mA
SCL						
V_{IL}	input voltage LOW		–0.3	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
f_{SCL}	clock frequency		0	–	100	kHz
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
C_I	input capacitance		–	–	10	pF
Inputs/outputs						
CRYSTAL OSCILLATOR (OSCIN; OSCOUT)						
f_{XTAL}	crystal frequency		–	27	–	MHz
G_v	small signal voltage gain		3.5	–	–	–
G_m	mutual conductance	f = 100 kHz	1.5	–	–	mA/V
C_I	input capacitance		–	–	10	pF
C_{FB}	feedback capacitance		–	–	5	pF
BLACK						
C_{blk}	storage capacitor to ground		–	100	–	nF
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
SDA						
V_{IL}	input voltage LOW		–0.3	–	1.5	V
V_{IH}	input voltage HIGH		3.0	–	V_{DD}+0.5	V
I_{LI}	input leakage current	V_I = 0 to V_{DD}	–10	–	10	µA
C_I	input capacitance		–	–	10	pF
t_r	input rise time	10% to 90%	–	–	2	µs
t_f	input fall time	90% to 10%	–	–	2	µs
V_{OL}	output voltage LOW	I_{OL} = 3 mA	0	–	0.5	V
t_f	output fall time	3 to 1 V	–	–	200	ns
C_L	load capacitance		–	–	400	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
STTV						
G_{stt}	gain of STTV relative to video input		0.9	1.0	1.1	
V_{tcs}	TCS amplitude		0.2	0.3	0.45	V
V_{DCs}	DC shift between TCS output and nominal video output		–	–	0.15	V
I_O	output drive current		–	–	3.0	mA
C_L	load capacitance		–	–	100	pF
R, G AND B						
V_{OL}	output voltage LOW	I_{OL} = 2 mA	0	–	0.2	V
V_{OH}	output voltage HIGH	I_{OH} = –1.6 mA; RGBREF ≤ V_{DD}–2 V	RGBREF –0.25 V	RGBREF	RGBREF +0.25 V	V
$\lvert Z_o \rvert$	output impedance		–	–	200	Ω
C_L	load capacitance		–	–	50	pF
I_{DC}	DC current		–	–	–3.3	mA
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
BLAN						
V_{OL}	output voltage LOW	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = –0.2 mA; V_{DD} = 4.5 V	1.1	–	–	V
V_{OH}	output voltage HIGH	I_{OH} = 0 mA; V_{DD} = 5.5 V	–	–	2.8	V
V_{OH}	allowed voltage at pin	with external pull-up	–	–	V_{DD}	V
C_L	load capacitance		–	–	50	pF
t_r	output rise time	10% to 90%	–	–	20	ns
t_f	output fall time	90% to 10%	–	–	20	ns
ODD/$\overline{\text{EVEN}}$						
V_{OL}	output voltage LOW	I_{OL} = 1.6 mA	0	–	0.4	V
V_{OH}	output voltage HIGH	I_{OH} = –1.6 mA	V_{DD}–0.4	–	V_{DD}	V
C_L	load capacitance		–	–	120	pF
t_r	output rise time	0.6 to 2.2 V	–	–	50	ns
t_f	output fall time	2.2 to 0.6 V	–	–	50	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
$\overline{COR}$ AND Y (OPEN DRAIN)						
V_{OH}	pull-up voltage at pin		–	–	V_{DD}	V
V_{OL}	output voltage LOW	I_{OL} = 5 mA	0	–	1.0	V
C_L	load capacitance		–	–	25	pF
t_f	output fall time	load resistor of 1.2 kΩ to V_{DD}; measured between V_{DD} −0.5 and 1.5 V	–	–	50	ns
I_{LO}	output leakage current	V_I = 0 to V_{DD}	−10	–	10	µA
T_{SK}	skew delay between display outputs R, G, B, $\overline{COR}$, Y and BLAN		–	–	20	ns
Timing						
I^2C-BUS						
t_{LOW}	clock LOW period		4	–	–	µs
t_{HIGH}	clock HIGH period		4	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		170	–	–	ns
$t_{SU;STO}$	set-up time from clock HIGH to STOP		4	–	–	µs
t_{BUF}	START set-up time following a STOP		4	–	–	µs
$t_{HD;STA}$	START hold time		4	–	–	µs
$t_{SU;STA}$	START set-up time following clock LOW-to-HIGH transition		4	–	–	µs

Notes to the characteristics

1. This current is the maximum allowed into the inputs when line and field flyback signals are connected to these inputs. Series current limiting resistors must be used to limit the input currents to ± 1 mA.
2. RGBREF is the positive supply for the RGB output pins and it must be able to source the I_{OH} current from the R, G and B pins. The leakage specification on RGBREF only applies when there is no current load on the RGB pins.

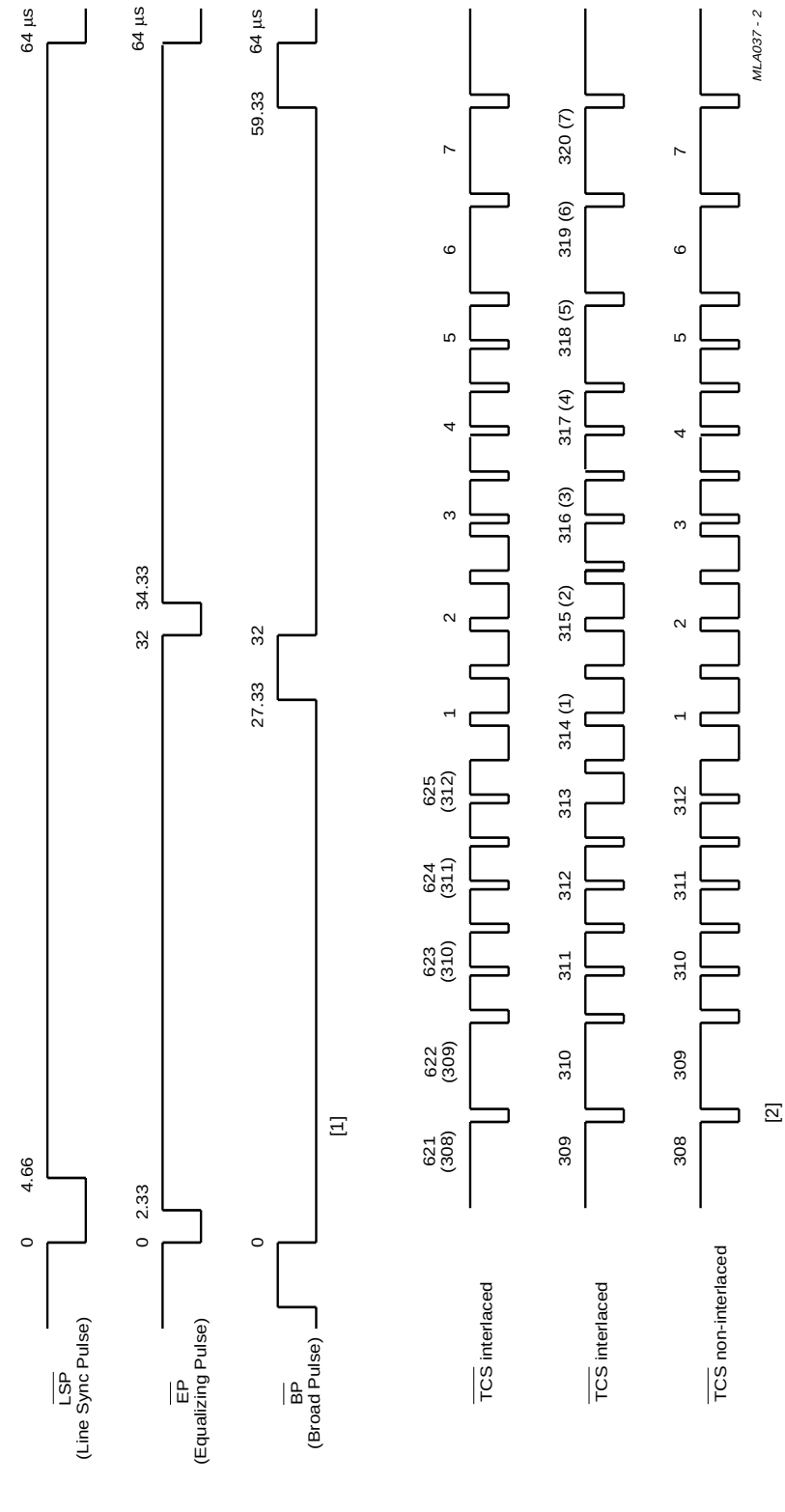
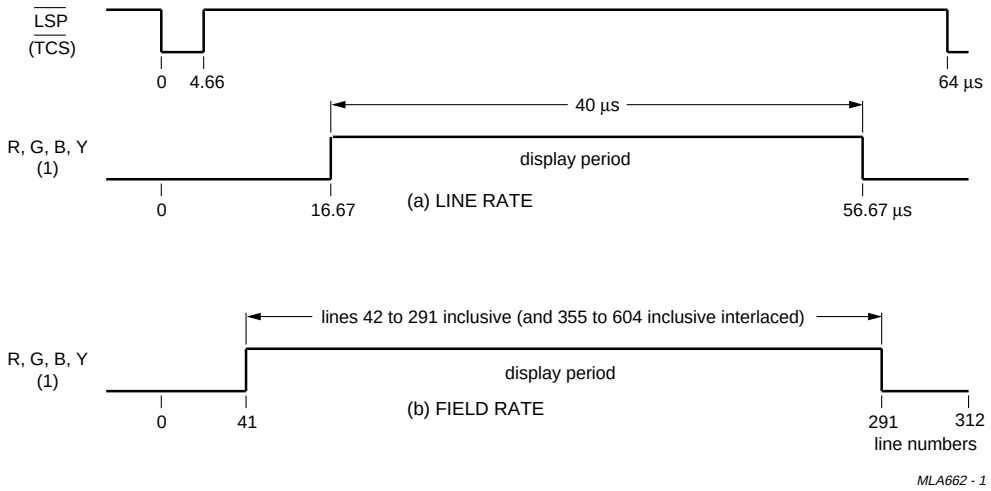


Fig.4 Composite sync waveforms.

[1] $\overline{LSP}$, $\overline{EP}$ and $\overline{BP}$ are combined to give $\overline{TCS}$ as shown below. All timings measured from falling edge of $\overline{LSP}$.

[2] Line numbers placed in the middle of the line. Equivalent count numbers in brackets.



(1) also BLAN in character and box blanking

Fig.5 Display output timing (a) line rate (b) field rate.

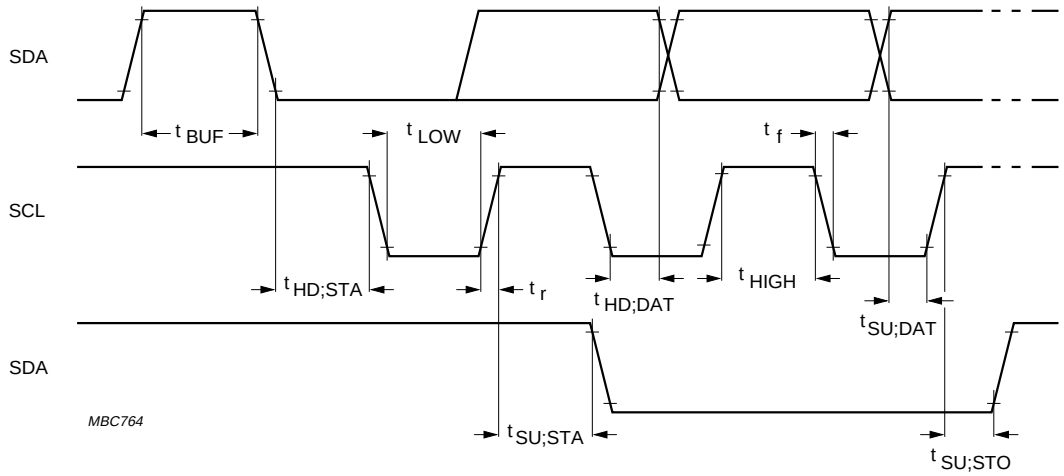
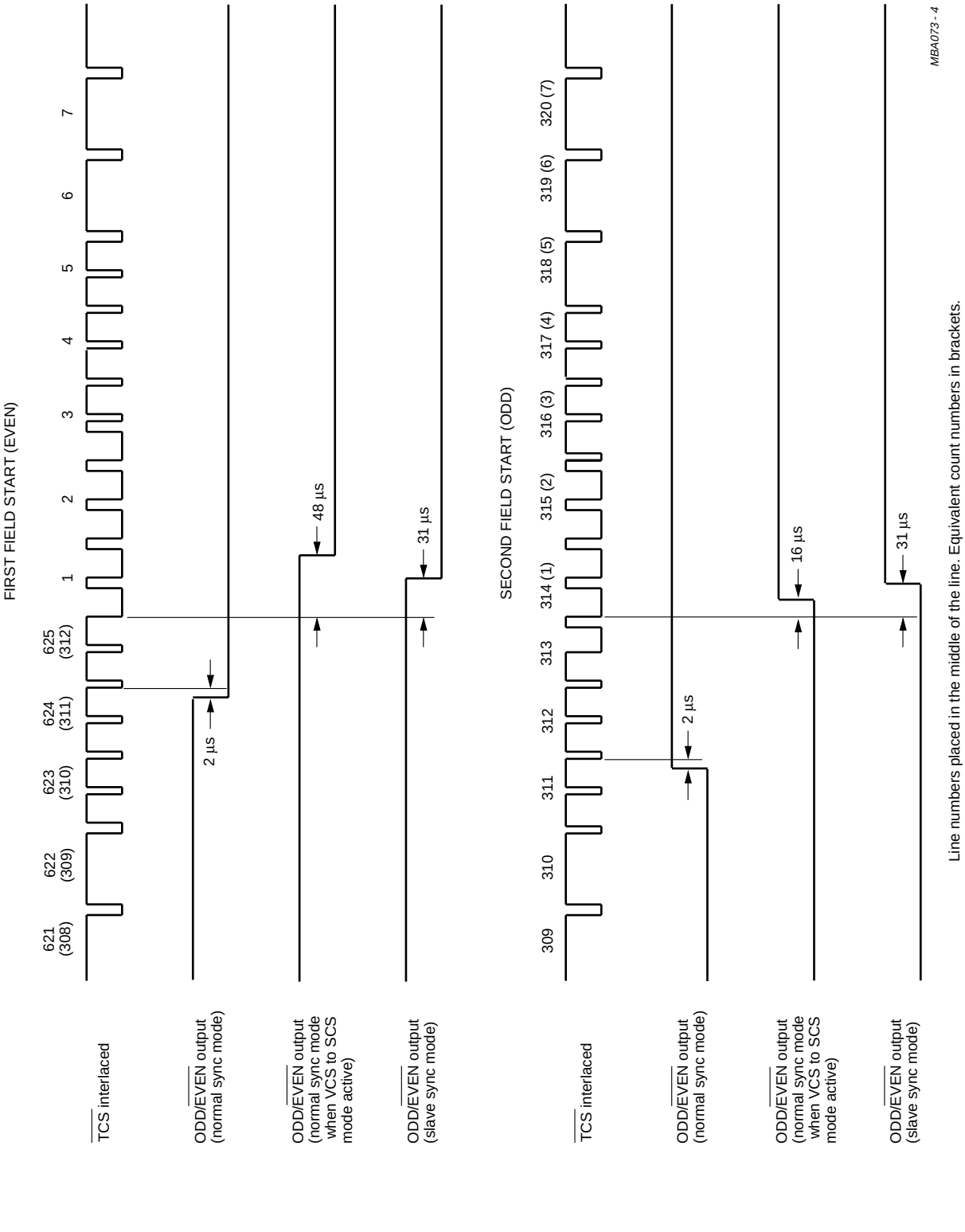


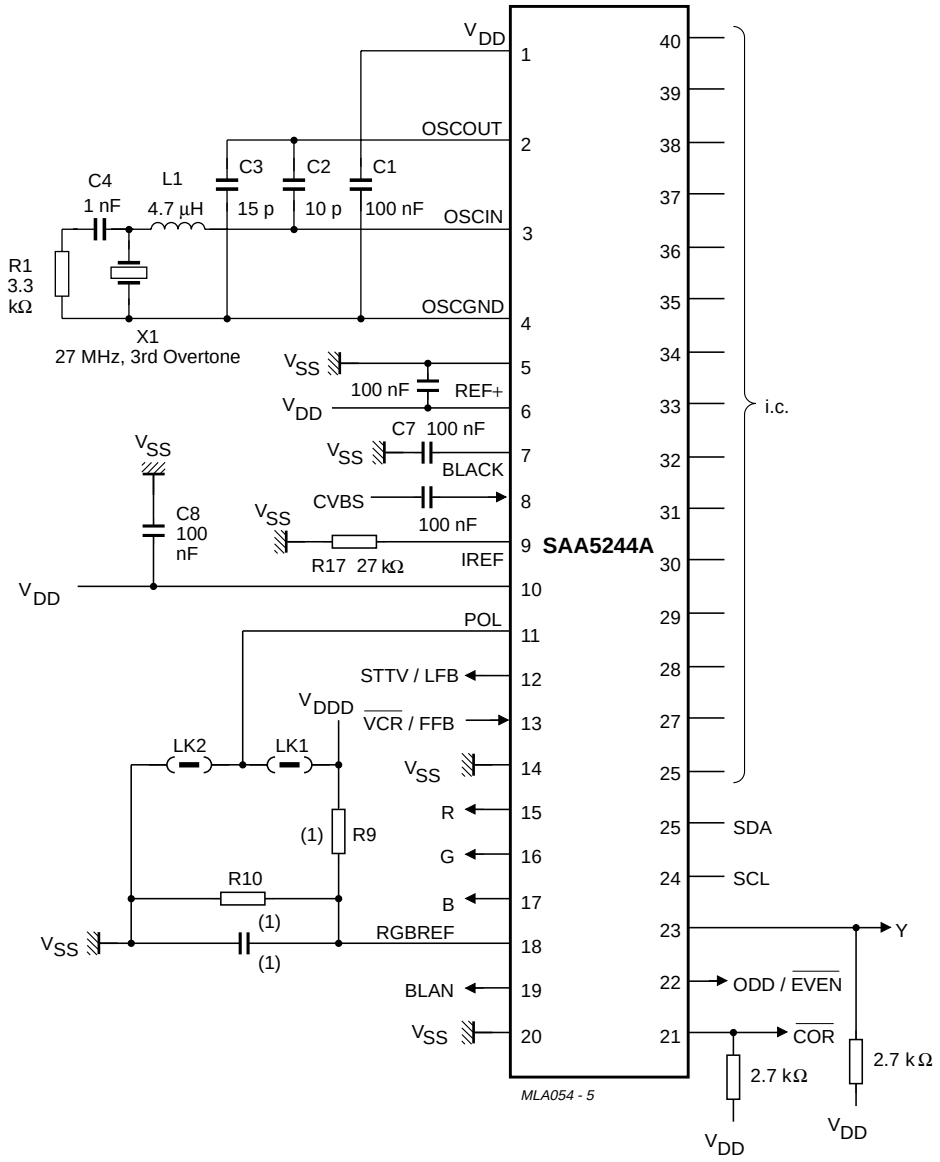
Fig.6 I²C-bus timing.



Line numbers placed in the middle of the line. Equivalent count numbers in brackets.

Fig.7 ODD/$\overline{\text{EVEN}}$ timing.

APPLICATION INFORMATION



(1) Value dependent on application.

Fig.8 Application diagram.

SAA5244A page memory organization

The organization of the page memory is shown in Fig.9. The device provides an additional row as compared with first generation decoders; this brings the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page; row 24 is available for software generated status messages and FLOF/FASTEXT prompt information.

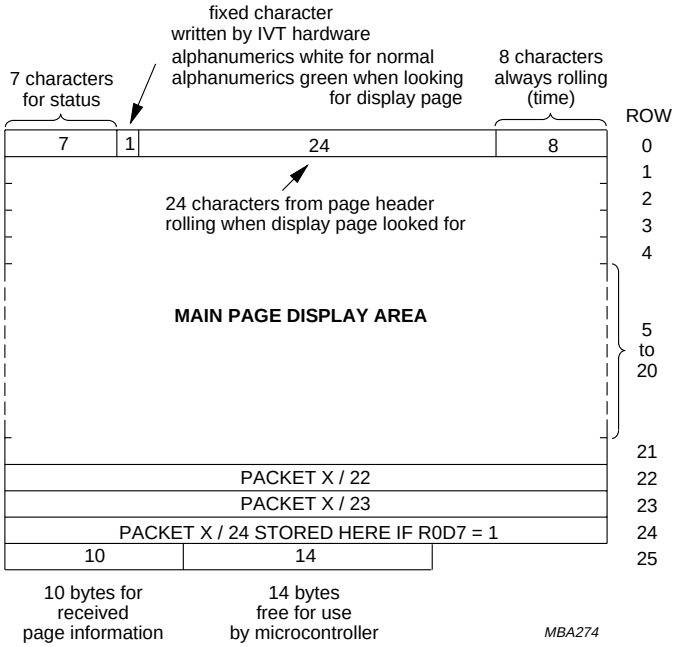


Fig.9 Basic page memory organization.

Row 0:

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by SAA5244A to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25:

The first 10 bytes of row 25 contain control data relating to the received page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

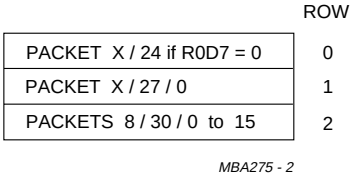


Fig.10 Organization of the extension memory.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

Page number	
MAG	magazine
PU	page units
PT	page tens
PBLF	page being looked for
$\overline{\text{FOUND}}$	LOW for page has been found
HAM.ER	Hamming error in corresponding byte
Page sub-code	
MU	minutes units
MT	minutes tens
HU	hours units
HT	hours tens
C4-C14	transmitted control bits.

Register maps

SAA5244A mode registers R0 to R11 are shown in Table 2. R0 to R10 are WRITE only; R11 is READ/WRITE. Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 Register map

REGISTER		D7	D6	D5	D4	D3	D2	D1	D0
Adv. control	0	X24 POS	FREE RUN PLL	AUTO ODD/$\overline{\text{EVEN}}$	DISABLE HDR ROLL	–	DISABLE ODD/$\overline{\text{EVEN}}$	–	$\overline{\text{R11}}$/R11B SELECT
Mode	1	VCS TO SCS	–	ACQ $\overline{\text{ON}}$/OFF	–	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0
Page request address	2	–	–	–	–	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0
Page request data	3	–	–	–	PRD4	PRD3	PRD2	PRD1	PRD0
		–	–	–	–	–	–	–	–
Display control (normal)	5	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display control (newsflash /subtitle)	6	BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN
Display mode	7	STATUS TOP	CURSOR ON	REVEAL ON	BOTTOM HALF	DOUBLE HEIGHT	BOX 24	BOX 1-23	BOX 0
		–	–	–	–	–	–	–	–
Cursor row	9	SUPPL. BLAST	CLEAR MEM.	A0	R4	R3	R2	R1	R0
Cursor column	10	SUPPL. ROW 24	SUPPL. ROW 0	C5	C4	C3	C2	C1	C0
Cursor data	11	–	D6	D5	D4	D3	D2	D1	D0
Device status	11B	$\overline{\text{625}}$/525 SYNC	ROM VER R4	ROM VER R3	ROM VER R2	ROM VER R1	ROM VER R0	TEXT SIGNAL QUALITY	VCS SIGNAL QUALITY

Notes to Table 2

1. '– ' indicates these bits are inactive and must be written to logic 0 for future compatibility.
2. All bits in registers R0 to R10 are cleared to logic 0 on power-up except bits D0 to D1 of registers R1, R5 and R6 which are set to logic 1.
3. All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha' white (00000111) as the acquisition circuit is enabled but the page is on hold.
4. TB must be set to logic 0 for normal operation.
5. The I^2C slave address is 0010001

REGISTER DESCRIPTION

R0 ADVANCED CONTROL - auto increments to Register 1

$\overline{R11}$/R11B SELECT	Selects reading of R11 or R11B
DISABLE ODD/$\overline{EVEN}$	Forces ODD/$\overline{EVEN}$ output LOW when logic 1
DISABLE HDR ROLL	Disables green rolling header and time
AUTO ODD/$\overline{EVEN}$	When set forces ODD/$\overline{EVEN}$ low if any TV picture displayed, if DISABLE ODD/$\overline{EVEN}$ = 0
FREE RUN PLL	Will force the PLL to free run in all conditions
X24 POS	Automatic display of FASTEXT prompt row when logic 1

R1 MODE - auto increments to Register 2

T0, T1	Interlace/non-interlace 312/313 line control (see Table 4)
TCS ON	Text composite sync or direct sync select
$\overline{DEW}$/FULL FIELD	Field-flyback or full channel mode
ACQ $\overline{ON}$/OFF	Acquisition circuits turned off when logic 1
VCS TO SCS	When logic 1 enables display of messages with 60 Hz input signal

R2 PAGE REQUEST ADDRESS - auto increments to Register 3

COL SC0 - SC2	Point to start column for page request data (see Table 3)
TB	Must be logic 0 for normal operation

R3 PAGE REQUEST DATA - does not auto increment (see Table 3)

R5 NORMAL DISPLAY CONTROL - auto increments to Register 6

R6 NEWSFLASH/SUBTITLE DISPLAY CONTROL - auto increments to Register 7

PON	Picture on
TEXT	Text on
COR	Contrast reduction on
BKGND	Background colour on

These functions have IN and OUT referring to inside and outside the boxing function respectively.

R7 DISPLAY MODE - does not auto increment

BOX ON 0	Boxing function allowed on Row 0
BOX ON 1-23	Boxing function allowed on Row 1-23
BOX ON 24	Boxing function allowed on Row 24
DOUBLE HEIGHT	To display double height text
BOTTOM HALF	To select bottom half of page when DOUBLE HEIGHT = 1
REVEAL ON	To reveal concealed text
CURSOR ON	To display cursor
STATUS TOP	Row 25 displayed above or below the main text

R9 CURSOR ROW - auto increments to Register 10

R0 to R4	Active row for data written to or read from memory via the I^2C-bus
A0	Selects display memory page (when = 0) or extension packet memory (when = 1)
CLEAR MEM.	When set to 1, clears the display memory. This bit is automatically reset
SUPPL. BLAST	When set to 1, column 4b and 5b (of Table 6) are mapped into 4 and 5 respectively, replacing blast-through alphanumerics in graphics mode

R10 CURSOR COLUMN - auto increments to Register 11 or 11B

C0 to C5	Active column for data written to or read from memory via the I^2C-bus
SUPPL. ROW 0	When set to 1, column 4b and 5b (of Table 6) are mapped into columns 6 and 7 respectively, just for row 0 columns 0 to 7
SUPPL. ROW 24	When set to 1, column 4b and 5b (of Table 6) are mapped into columns 6 and 7 respectively just for row 24

R11 CURSOR DATA - does not auto increment

D0 to D6	Data read from/written to memory via I^2C, at location pointed to by R9 and R10. This location automatically increments each time R11 is accessed

R11B DEVICE STATUS - does not auto increment

VCS SIGNAL QUALITY	Indicates that the video signal quality is good and PLL is phase locked to input video when = 1
TEXT SIGNAL QUALITY	If a good teletext signal is being received when = 1
ROM VER R0 to R4	Indicated language/ROM variant. For Western European = 01000
$\overline{625}$/525 SYNC	If the input video is a 525 line signal when = 1

Table 3 Register map for page requests (R3)

START COLUMN	PRD4	PRD3	PRD2	PRD1	PRD0
0	Do care Magazine	$\overline{\text{HOLD}}$	MAG2	MAG1	MAG0
1	Do care Page tens	PT3	PT2	PT1	PT0
2	Do care Page units	PU3	PU2	PU1	PU0
3	Do care Hours tens	X	X	HT1	HT0
4	Do care Hours units	HU3	HU2	HU1	HU0
5	Do care Minutes tens	X	MT2	MT1	MT0
6	Do care Minutes units	MU3	MU2	MU1	MU0

Notes to Table 3

1. Abbreviations are as for Table 1 except for DO CARE bits.
2. When the DO CARE bit is set to logic 1 this means the corresponding digit is to be taken into account for page requests. If the DO CARE bit is set to logic 0 the digit is ignored. This allows, for example, ‘normal’ or ‘timed page’ selection.
3. If $\overline{\text{HOLD}}$ is set LOW, the page is held and not updated.
4. Columns auto-increment on successive I^2C-bus transmission bytes.

Table 4 Interlace/non-interlace 312/313 line control (T0 and T1)

T1	T0	RESULT
0	0	interlaced 312.5/312.5 lines
0	1	non-interlaced 312/313 lines (note 1)
1	0	non-interlaced 312/312 lines (note 1)
1	1	scan-locked

Note to Table 4

1. Reverts to interlaced mode if a newsflash or subtitle is being displayed.

Table 5 Crystal characteristics

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Crystal (27 MHz, 3rd overtone)					
C1	series capacitance	–	1.7	–	pF
C0	parallel capacitance	–	5.2	–	pF
C_L	load capacitance	–	20	–	pF
Rr	resonant resistance	–	–	50	Ω
R1	series resistance	–	20	–	Ω
Xa	ageing	–	–	±5	10^{-6}/yr
Xj	adjustment tolerance	–	–	±25	10^{-6}
Xd	drift	–	–	±25	10^{-6}

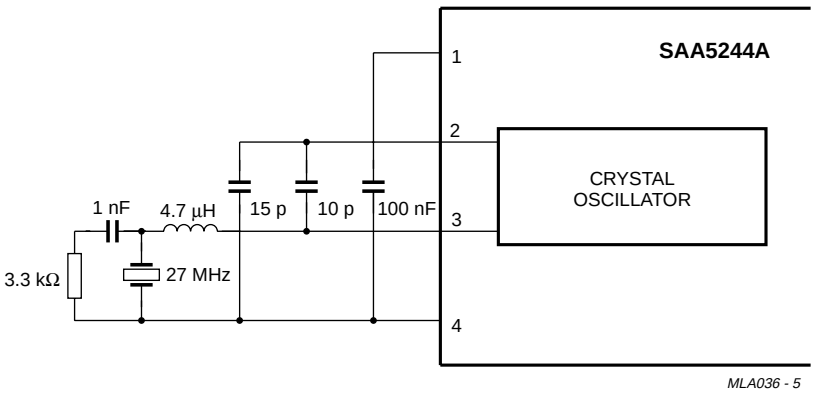


Fig.11 Crystal oscillator application diagram.

CLOCK SYSTEMS

Crystal oscillator

The crystal is a conventional 2-pin design operating at 27 MHz. It is capable of oscillating with both fundamental and third overtone mode crystals. External components should be used to suppress the fundamental output of the third overtone, as shown in Fig.11. The crystal characteristics are given in Table 5.

Character sets

The WST specification allows the selection of national character sets via the page header transmission bits, C12 to C14. The basic 96 character sets differ only in 13 national option characters as indicated in Table 8 with reference to their table position in the basic character matrix illustrated in Table 7. The SAA5244A automatically decodes transmission bits C12 to C14. Table 6 illustrates the character matrices.

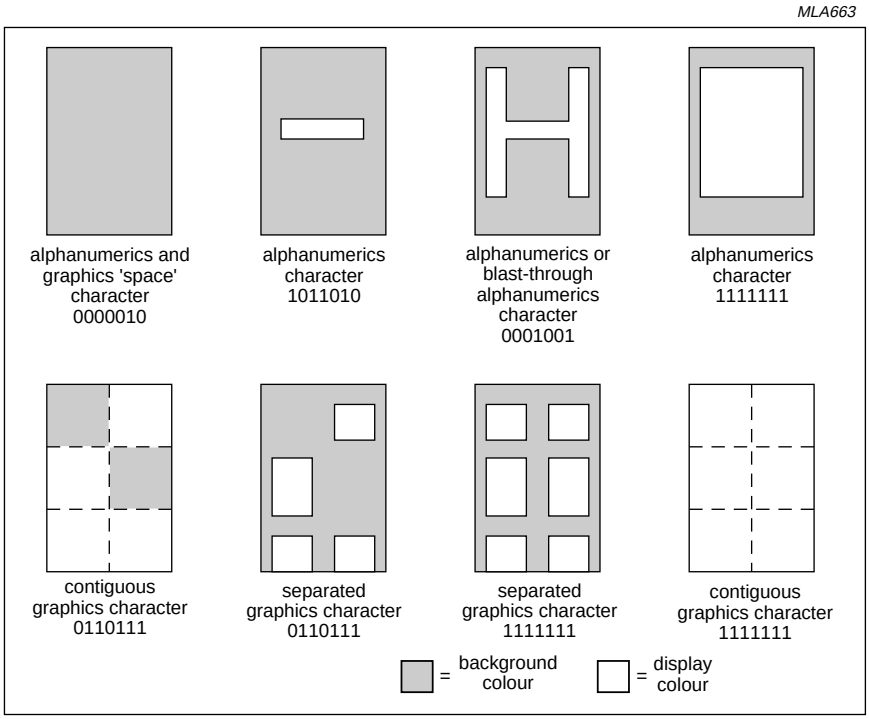


Fig.12 Character format.

Table 6 SAA5244P/A character data input decoding

BITS b_7 b_6 b_5				0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1	AVAILABLE AS NATIONAL OPTIONS ONLY			
b_4	b_3	b_2	b_1	column 0	1	2	2a	3	3a	4	4b +	5	5b +	6	6a	7	7a				
0	0	0	0	0	alpha - numerics black	graphics black															
0	0	0	1	1	alpha - numerics red	graphics red															
0	0	1	0	2	alpha - numerics green	graphics green															
0	0	1	1	3	alpha - numerics yellow	graphics yellow															
0	1	0	0	4	alpha - numerics blue	graphics blue															
0	1	0	1	5	alpha - numerics magenta	graphics magenta															
0	1	1	0	6	alpha - numerics cyan	graphics cyan															
0	1	1	1	7	alpha - numerics white **	graphics white															
1	0	0	0	8	flash	conceal display															
1	0	0	1	9	steady **	contiguous graphics **															
1	0	1	0	10	end box **	separated graphics															
1	0	1	1	11	start box	ESC *															
1	1	0	0	12	normal hight **	black back - ground **															
1	1	0	1	13	double height	new back - ground															
1	1	1	0	14	SO *	hold graphics															
1	1	1	1	15	SI *	release graphics **															

MBA266 - 1

Notes to Table 6 **- For character version number (01000) see Register 11B**

1. ***** These control characters are reserved for compatibility with other data codes.
2. ****** These control characters are presumed before each row begins.
3. **+** Columns 4b and 5b can only be accessed when supplementary character bits are set (see Registers 9 and 10).
4. Control characters shown in columns 0 and 1 are normally displayed as spaces.
5. Characters may be referred to by column and row, For example 2/5 refers to %.

6. Black represents displayed colour. White represents background.
7. Character rectangle shown as follows:
8. The SAA5244A national option characters are illustrated in Table 8.
9. Characters 4b/11, 4b/12, 5b/10, 5b/11 and 5b/12 are special characters for combining with character 4b/10.
10. National option characters will be developed according to the setting of control bits C12 to C14. These will be mapped into the basic code table into positions shown in Table 8.
11. Columns 4b and 5b are mapped into 4 and 5 respectively (replacing blast-through alphanumerics in the graphics mode) when enabled by R9 bit D7 set to 1.
12. Columns 4b and 5b are mapped into columns 6 and 7 respectively when enabled by R10 bit D6 (row 0 columns 0 to 7) and R10 bit D7 (row 24) set to 1.
13. Columns 2a, 3a, 6a and 7a are displayed in graphics mode.

Table 7 SAA5244A Basic character matrix

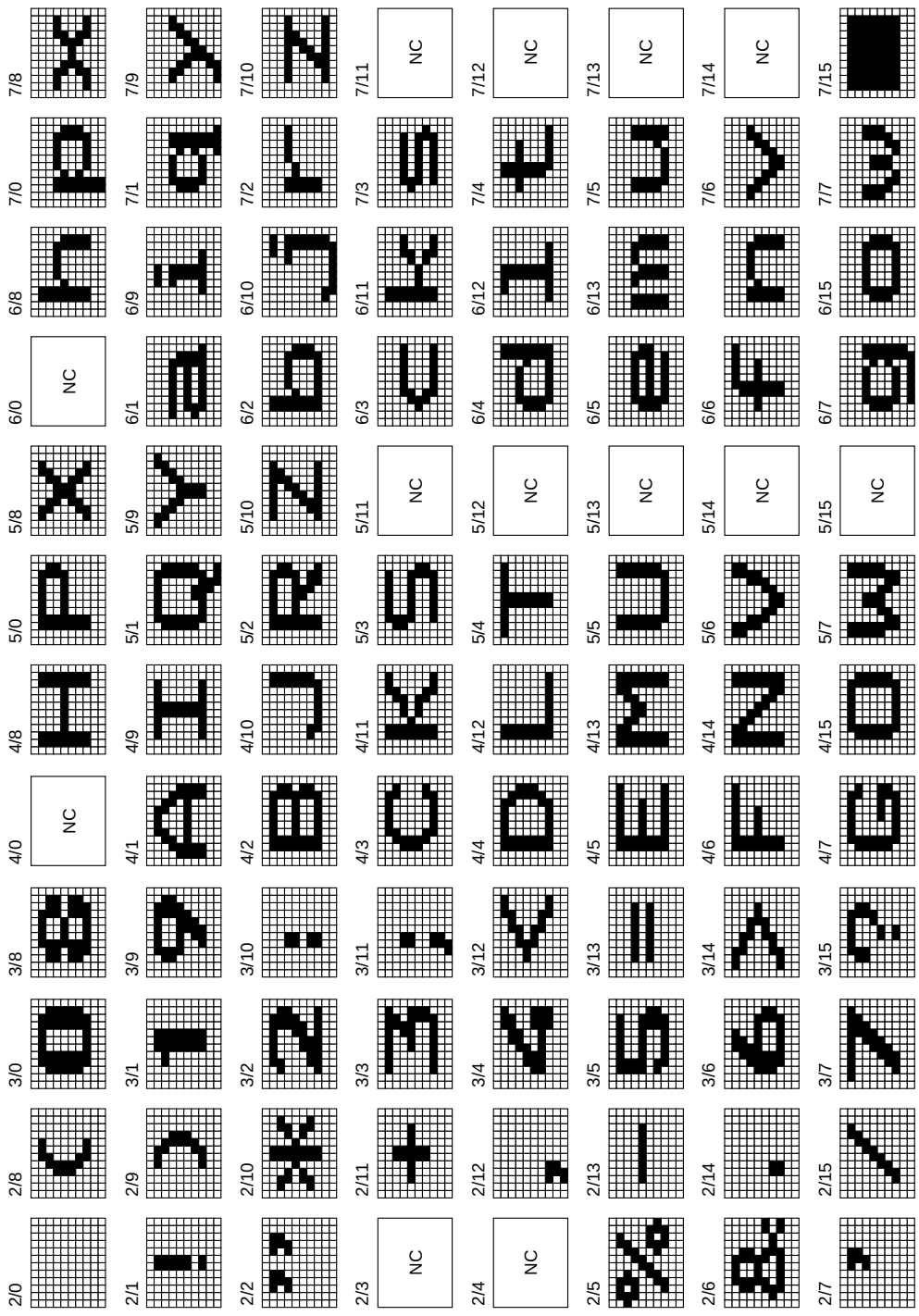


Table 8 SAA5244A national option character set

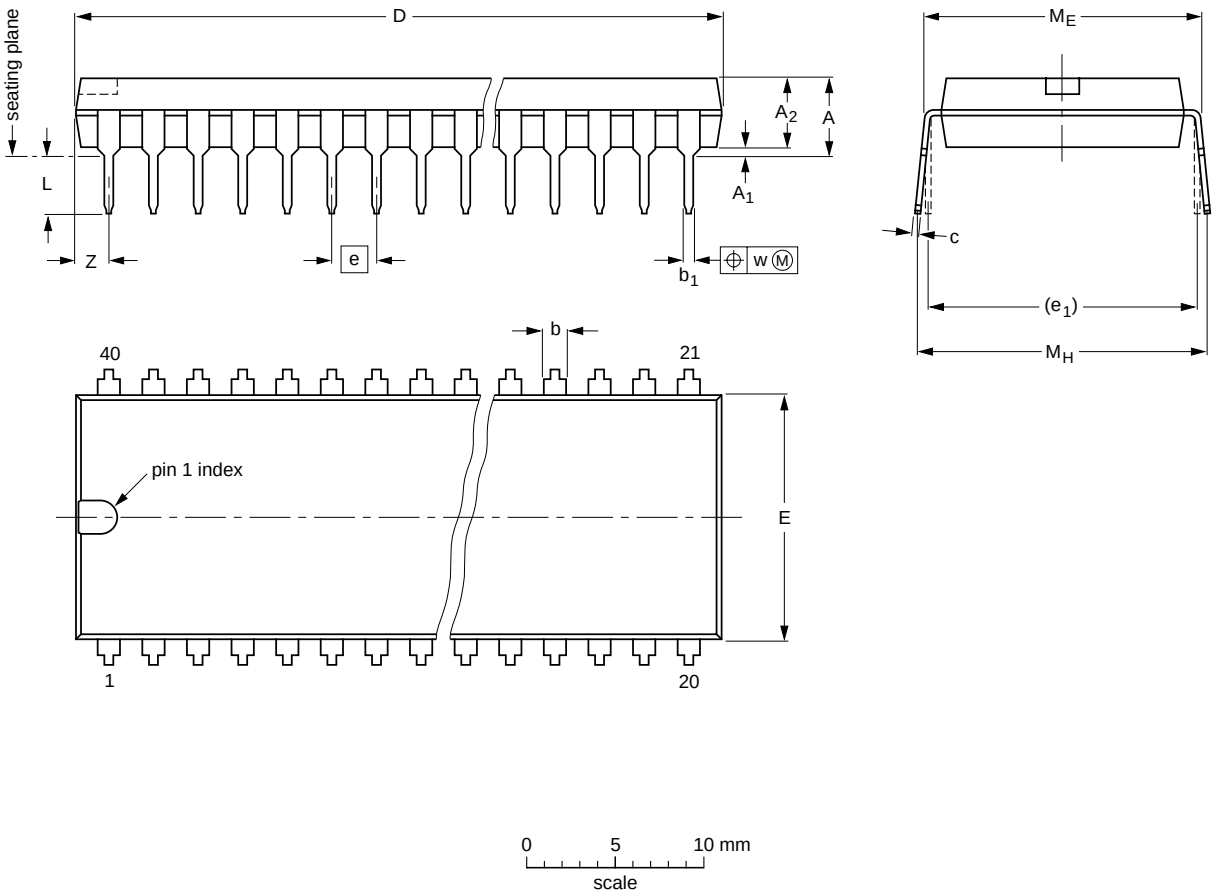
LANGUAGE	PHCB (1)			CHARACTER POSITION (COLUMN / ROW)													
	C12	C13	C14	**2 / 3**	**2 / 4**	**4 / 0**	**5 / 11**	**5 / 12**	**5 / 13**	**5 / 14**	**5 / 15**	**6 / 0**	**7 / 11**	**7 / 12**	**7 / 13**	**7 / 14**
ENGLISH	**0**	**0**	**0**	£	$	@	←	½	→	↑	#	—	¼	‖	¾	÷
GERMAN	**0**	**0**	**1**	#	$	§	Ä	Ö	Ü	^	_	°	ä	ö	ü	ß
SWEDISH	**0**	**1**	**0**	#	¤	É	Ä	Ö	Å	Ü	_	é	ä	ö	å	ü
ITALIAN	**0**	**1**	**1**	£	$	é	°	ç	→	↑	#	ù	à	ò	è	ì
FRENCH	**1**	**0**	**0**	é	ï	à	ë	ê	ù	î	#	è	â	ô	û	ç

MLA664

(1) PHCB are the Page Header Control Bits. Other combinations default to English.

PACKAGE OUTLINES

DIP40: plastic dual in-line package; 40 leads (600 mil) **SOT129-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

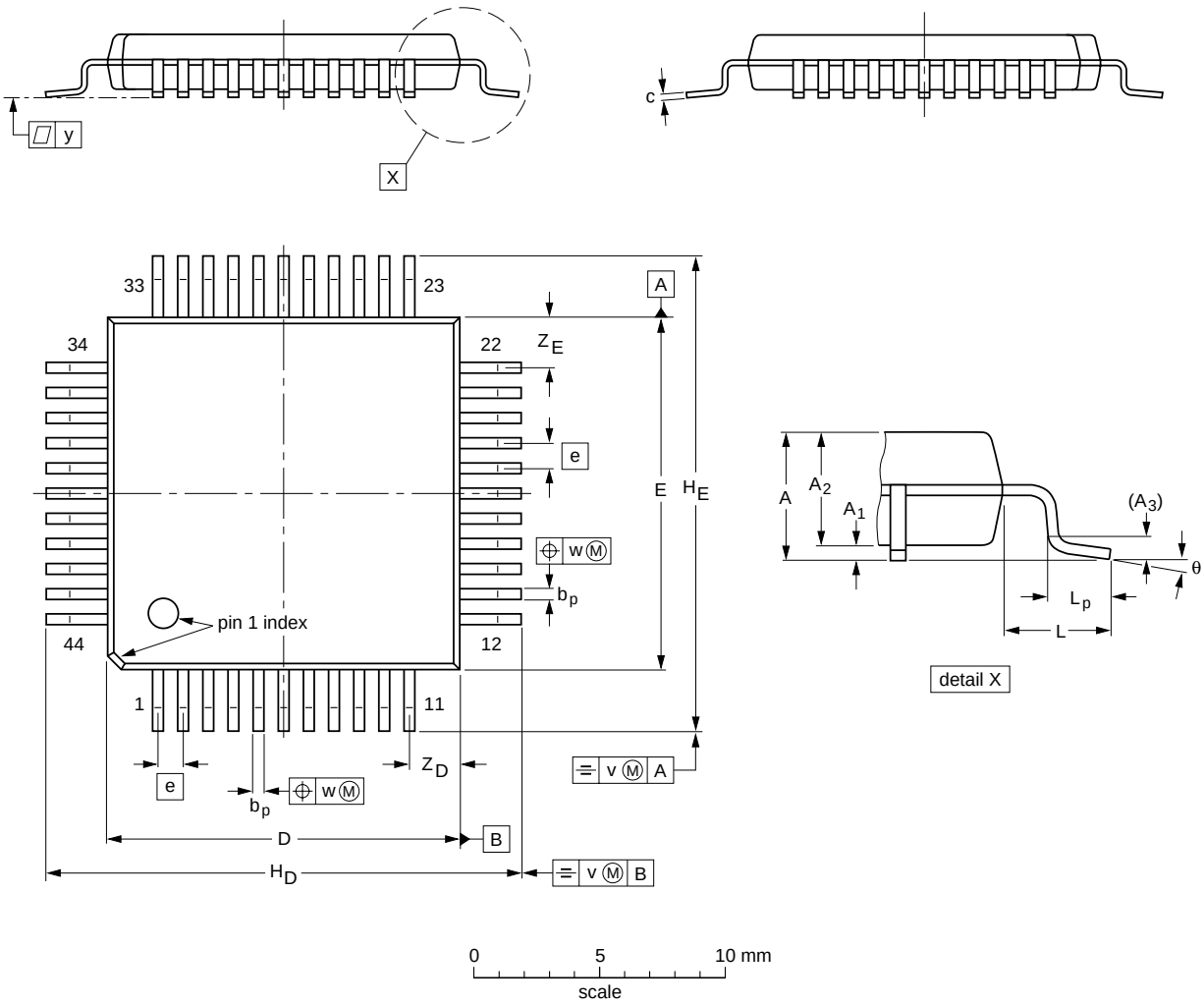
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	4.0	1.70 1.14	0.53 0.38	0.36 0.23	52.50 51.50	14.1 13.7	2.54	15.24	3.60 3.05	15.80 15.24	17.42 15.90	0.254	2.25
inches	0.19	0.020	0.16	0.067 0.045	0.021 0.015	0.014 0.009	2.067 2.028	0.56 0.54	0.10	0.60	0.14 0.12	0.62 0.60	0.69 0.63	0.01	0.089

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT129-1	051G08	MO-015AJ				~~92-11-17~~ 95-01-14

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm **SOT205-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01A					~~95-02-04~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

QFP

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary from 50 to 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheat for 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.